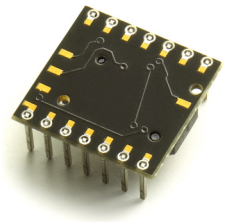
ADNS-6530
Integrated COB LaserStream sensor

Data Sheet

Lead (Pb) Free
RoHS 6 fully
compliant



Description

The Avago Technologies ADNS-6530 integrated Chip-con-board (COB) LaserStream sensor along with the ADNS-6150 (SFF) lens form a complete and compact laser mouse tracking system. It is the laser-illuminated small form factor (SFF) navigation system. Targeted at cordless applications. The chip integrates the sensor and VCSEL into a single package, providing a small form factor. This new opto-mechanical architecture allows for more compact and cost-effective mouse designs. Powered by latest Avago Technologies LaserStreamTM engine, the mouse can track on more than traditional LED-based optical navigation, especially on glossy and reflective ones. In addition, the high-performance, low power architecture is capable of sensing high-speed mouse motion while prolonging battery life-two performance areas essential in demanding cordless applications.

There is no moving part in the complete assembly for ADNS-6530 laser mouse system, thus it is high reliability and less maintenance for the end user. In addition, precision optical alignment is not required, facilitating high volume assembly.

Theory of Operation

The ADNS-6530 integrated COB LaserStream sensor comprises of sensor and VCSEL in a single package.

The advanced class of VCSEL was engineered by Avago Technologies to provide a laser diode with a single longitudinal and a single transverse mode. In contrast to most oxide-based single-mode VCSEL, this class of Avago Technologies VCSEL remains within single mode operation over a wide range of output power. It has significantly lower power consumption than a LED. It is an excellent choice for optical navigation applications.

The sensor is based on LaserStream™ technology, which measures changes in position by optically acquiring sequential surface images (frames) and mathematically determining the direction and magnitude of movement. It contains an Image Acquisition System (IAS), a Digital Signal Processor (DSP), and a four wire serial port. The IAS acquires microscopic surface images via the lens and illumination system. These images are processed by the DSP to determine the direction and distance of motion. The DSP calculates the Δx and Δy relative displacement values. An external microcontroller reads the Δx and Δy information from the sensor serial port. The microcontroller then translates the data into PS2, USB, or RF signals before sending them to the host PC or game console.

Features

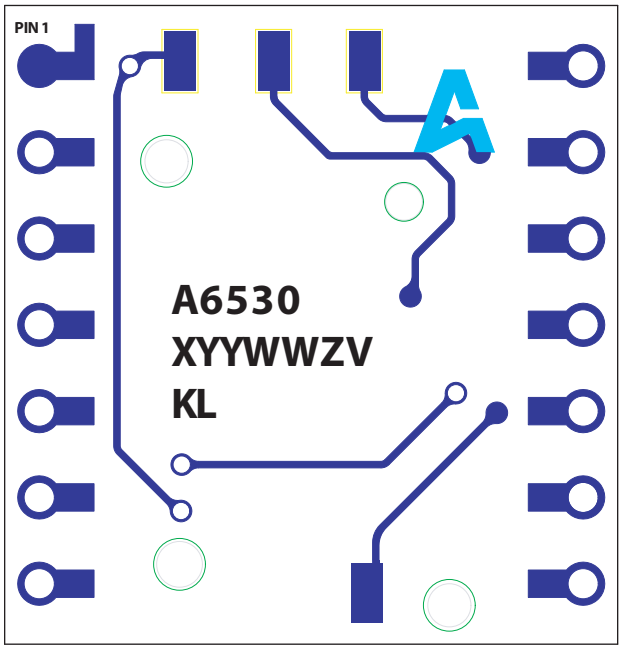
- Small form factor, integrated chip-on-board package
- Low power architecture
- New LaserStream technology
- Self-adjusting power-saving modes for longest battery life
- High speed motion detection up to 20 ips and 8g
- Enhanced SmartSpeed self-adjusting frame rate for optimum performance
- Motion detect pin output
- Internal oscillator – no clock input needed
- Selectable 400 and 800 cpi resolution
- Wide operating voltage: 2.7V-3.6V nominal
- Four wire serial port
- Minimal number of passive components
- Laser fault detect circuitry on-chip for Eye Safety Compliance
- Advanced Technology VCSEL chip
- Single Mode Lasing operation
- 832-865 nm wavelength

Applications

- Laser Mice
- Optical trackballs
- Integrated input devices
- Battery-powered input devices

Pinout of ADNS-6530 Optical Mouse Sensor

Pin	Name	Description
1	-VCSEL	Negative Terminal of VCSEL
2	NCS	Chip select (active low input)
3	MISO	Serial data output (Master In/Slave Out)
4	SCLK	Serial clock input
5	MOSI	Serial data input (Master Out/Slave In)
6	MOTION	Motion Detect (active low output)
7	LASER_NEN	LASER Enable (Active LOW)
8	AVDD	Analog Supply Voltage
9	AGND	Analog Ground
10	GND	Ground
11	GND	Ground
12	GND	Ground
13	VDD	Supply Voltage
14	+VCSEL	Positive Terminal of VCSEL



X = Subcon code
YYWW = Date code
Z = Sensor Die Source
V = VCSEL Die Source
KL = VCSEL Binning (2A, 3A)

Figure 1. Package outline drawing (top view)

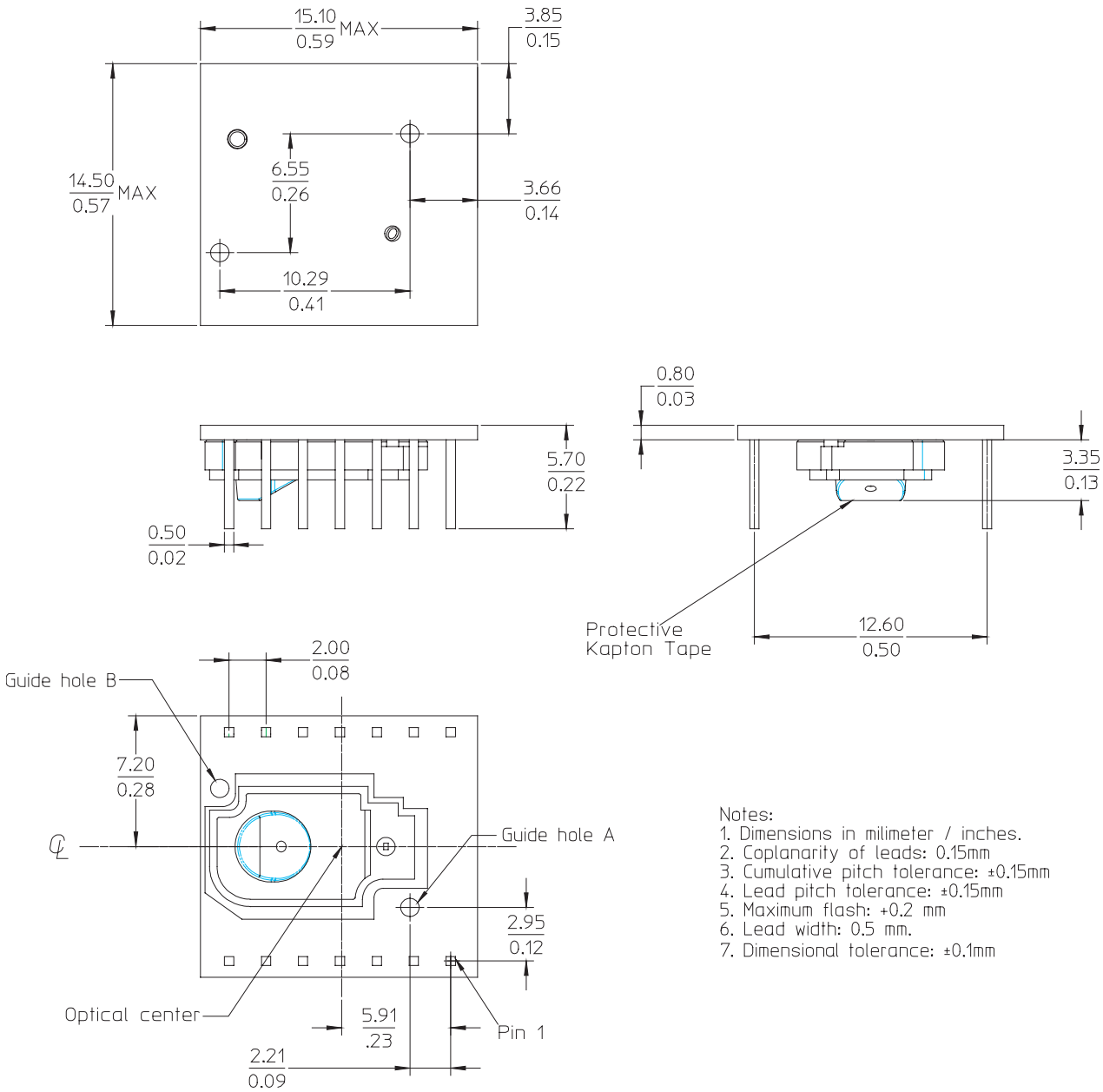


Figure 2. Package outline drawing

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD

Overview of Laser Mouse Sensor Assembly

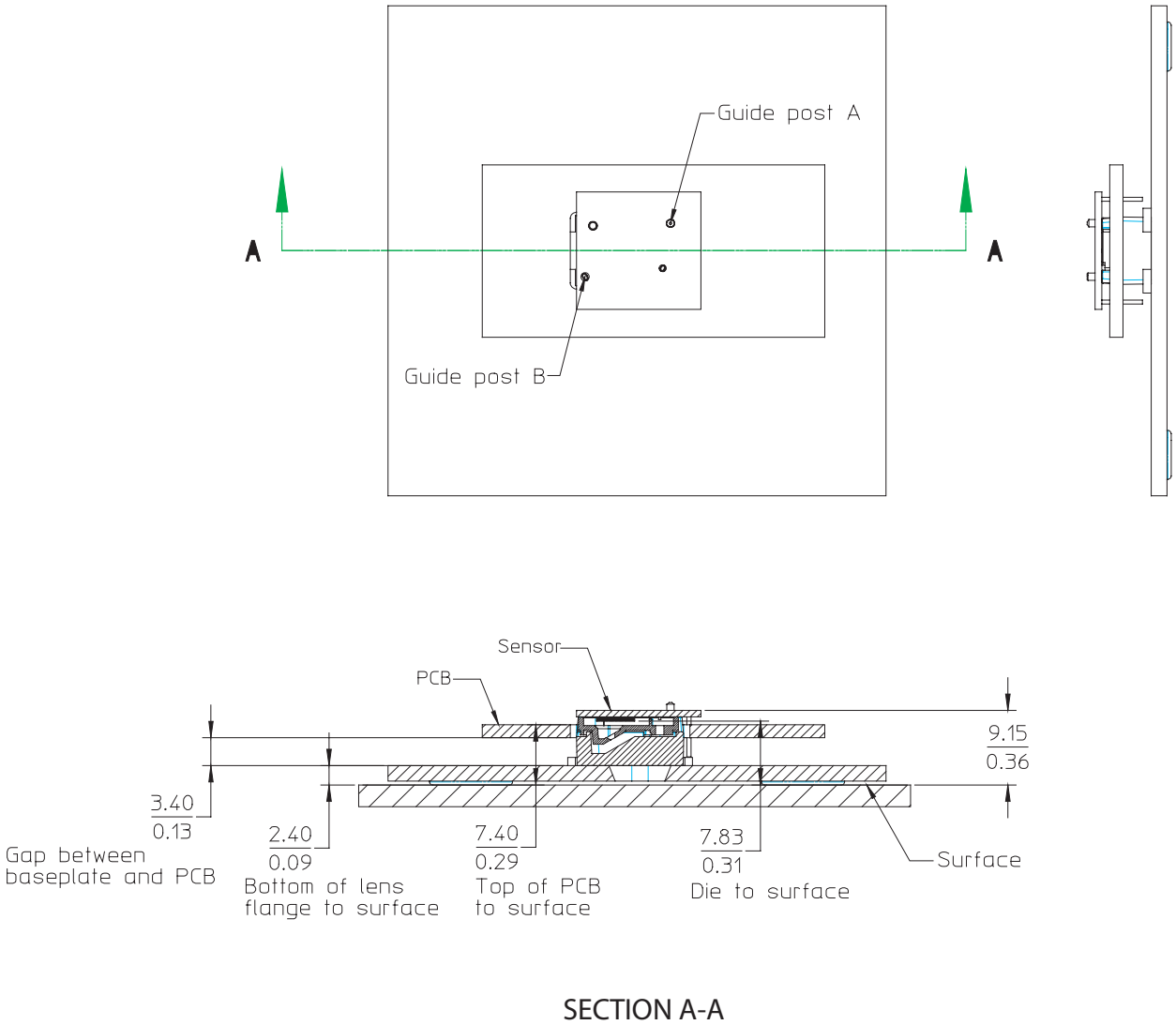


Figure 3. 2D Assembly Drawing of ADNS-6530, PCBs and Base Plate

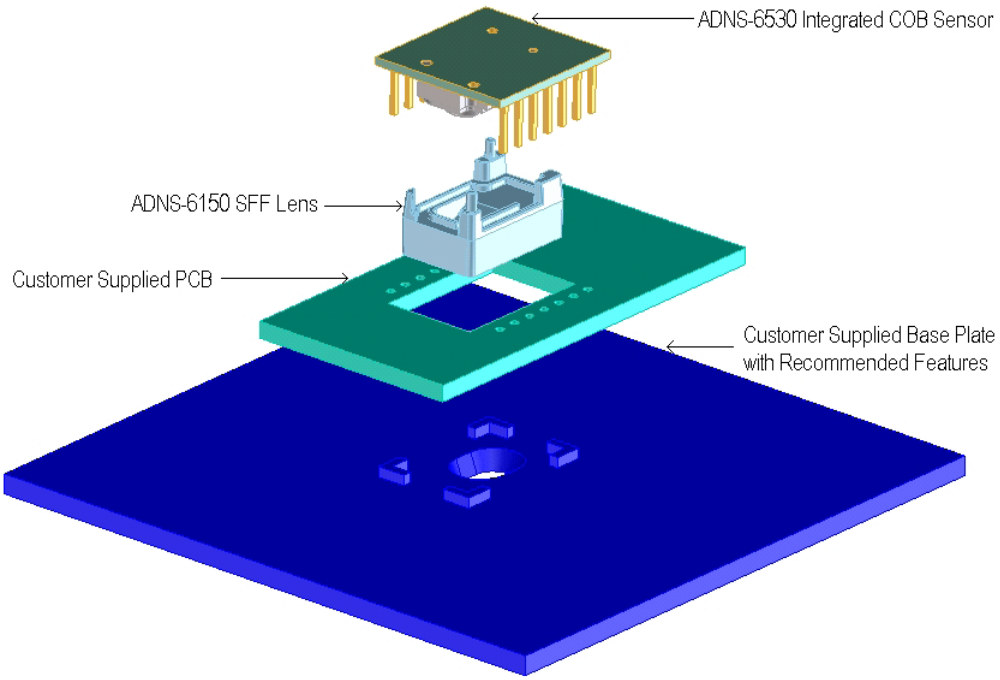


Figure 4. Exploded view drawing

Shown with ADNS-6530 integrated COB LaserStream sensor and ADNS-6150 SFF lens, the components self-align as they are mounted onto defined features on the base plate.

The ADNS-6530 integrated COB LaserStream sensor is designed for mounting on a through-hole PCB, looking down. There are an aperture stop and guide holes on the package that align to the ADNS-6150 SFF lens.

The VCSEL is used for illumination, provides a laser diode with a single longitudinal and a single transverse mode. It is particularly suited as lower power consumption and highly coherent replacement of LEDs. It also provides wider operation range while still remaining within single-mode, reliable operating conditions.

The ADNS-6150 SFF lens is designed for use with ADNS-6530 integrated COB LaserStream sensor. The VCSEL contained in the package and the lens provides the directed illumination and optical imaging necessary for proper operation of the sensor. ADNS-6150 SFF lens is precision molded optical components and should be handled with care to avoid scratching of the optical surfaces.

Avago Technologies provides a STEP or IGES file drawing describing the base plate molding features for lens and PCB alignment.

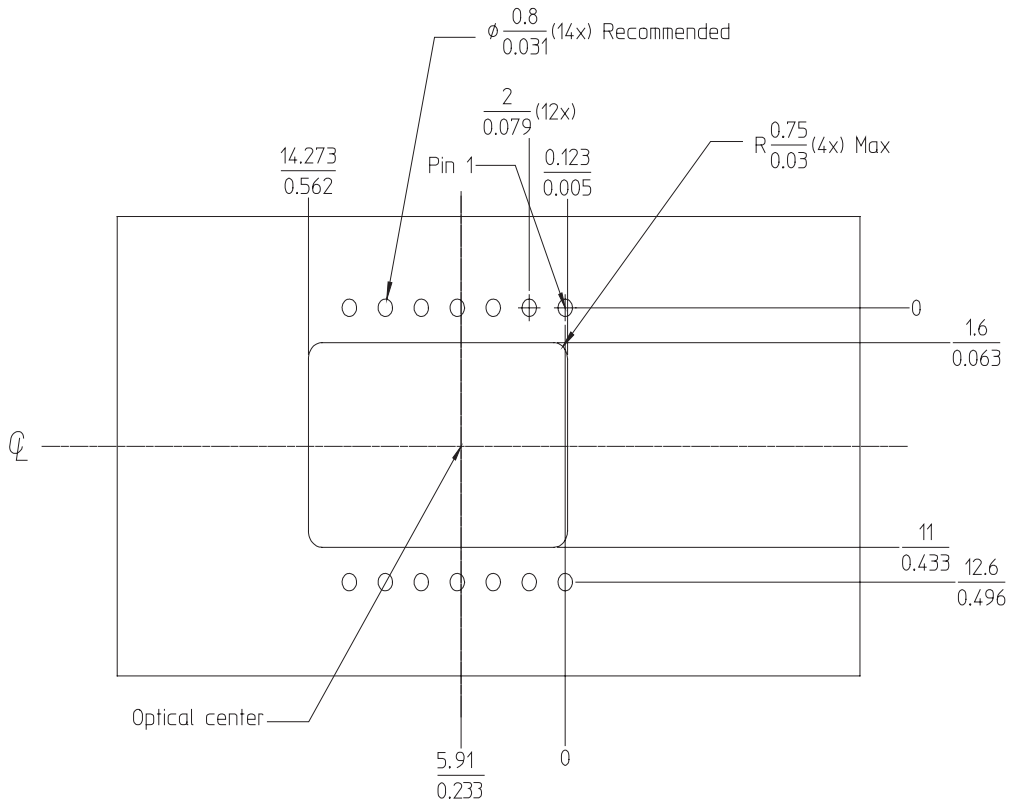


Figure 5. Recommended PCB mechanical cutouts and spacing

Assembly Recommendation

1. Insert the integrated COB LaserStream sensor and all other electrical components into the application PCB.
2. Wave-solder the entire assembly in a no-wash solder process utilizing a solder fixture. The solder fixture is needed to protect the sensor during the solder process. It also sets the correct sensor-to-PCB distance, as there is no stopper feature on the lead to rest the package on the PCB surface. The fixture should be designed to expose the sensor leads to solder while shielding the optical aperture from direct solder contact.
3. Place the lens onto the base plate. Care must be taken to avoid contamination on the optical surfaces.
4. Remove the protective kapton tapes from the optical apertures of the sensor and VCSEL respectively. Care must be taken to keep contaminants from entering the apertures.
5. Insert the PCB assembly over the lens onto the base plate. The sensor package should self-align to the lens. The optical position reference for the PCB is set by the base plate and lens. The alignment guide post of the lens locks the lens and integrated COB LaserStream sensor together. Note that the PCB motion due to button presses must be minimized to maintain optical alignment.
6. Optional: The lens can be permanently locked to the sensor package by melting the lens' guide posts over the sensor with heat staking process.
7. Tune the laser output power from the VCSEL to meet the Eye Safe Class I Standard as detailed in the LASER Power Adjustment Procedure.
8. Install the mouse top case. There must be a feature in the top case (or other area) to press down onto the sensor to ensure the sensor and lens are interlocked to the correct vertical height.

Design considerations for improving ESD Performance

For improved electrostatic discharge performance, typical creepage and clearance distance are shown in the table below. Assumption: base plate construction as per the Avago Technologies supplied STEP or IGES file and ADNS-6150 lens:

Typical Distance	Millimeters
Creepage	12.1*
Clearance	2.0

* Inclusive of the 2.4mm typical distance from lens reference plane to surface, Z (equivalent to baseplate and foot-pads thickness). Exclusive of the 2.4mm, creepage = 9.7mm

Note that the lens material is polycarbonate and therefore, cyanoacrylate based adhesives or other adhesives that may damage the lens should NOT be used.

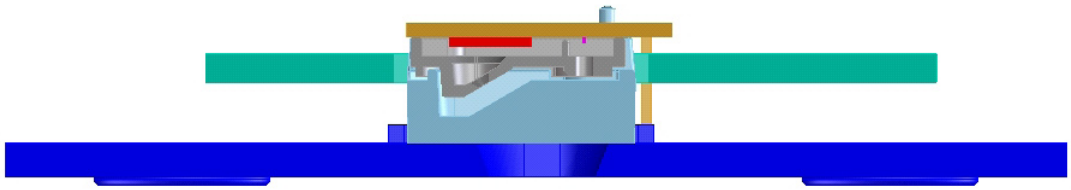


Figure 6. Sectional view of PCB assembly highlighting optical mouse components

Application Circuit

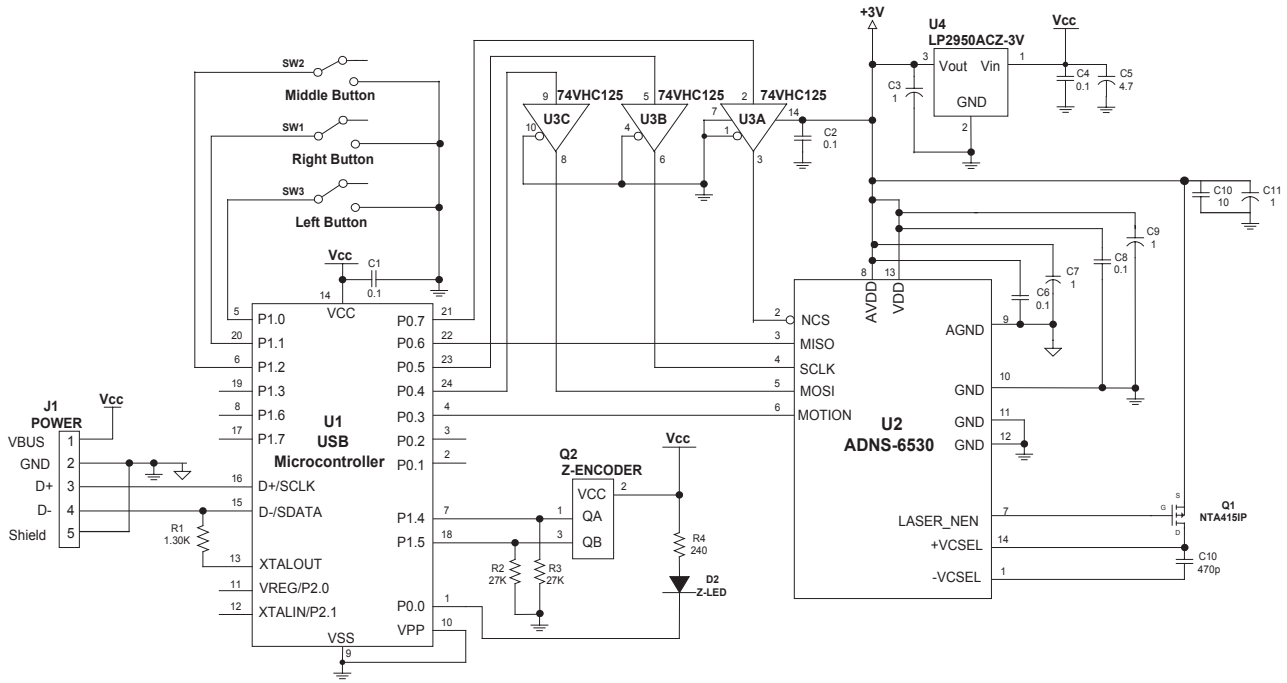


Figure 7a. Schematic Diagram for 3-Button Scroll Wheel Corded Mouse

Notes

- The supply and ground paths should be laid out using a star methodology.
- Level shifting is required to interface a 5V micro-controller to the ADNS-6530. If a 3V micro-controller is used, the 74VHC125 component shown may be omitted.
- All the caps must be placed as near as possible to the ADNS-6530, micro-controller and RF ICs for noise filtering.

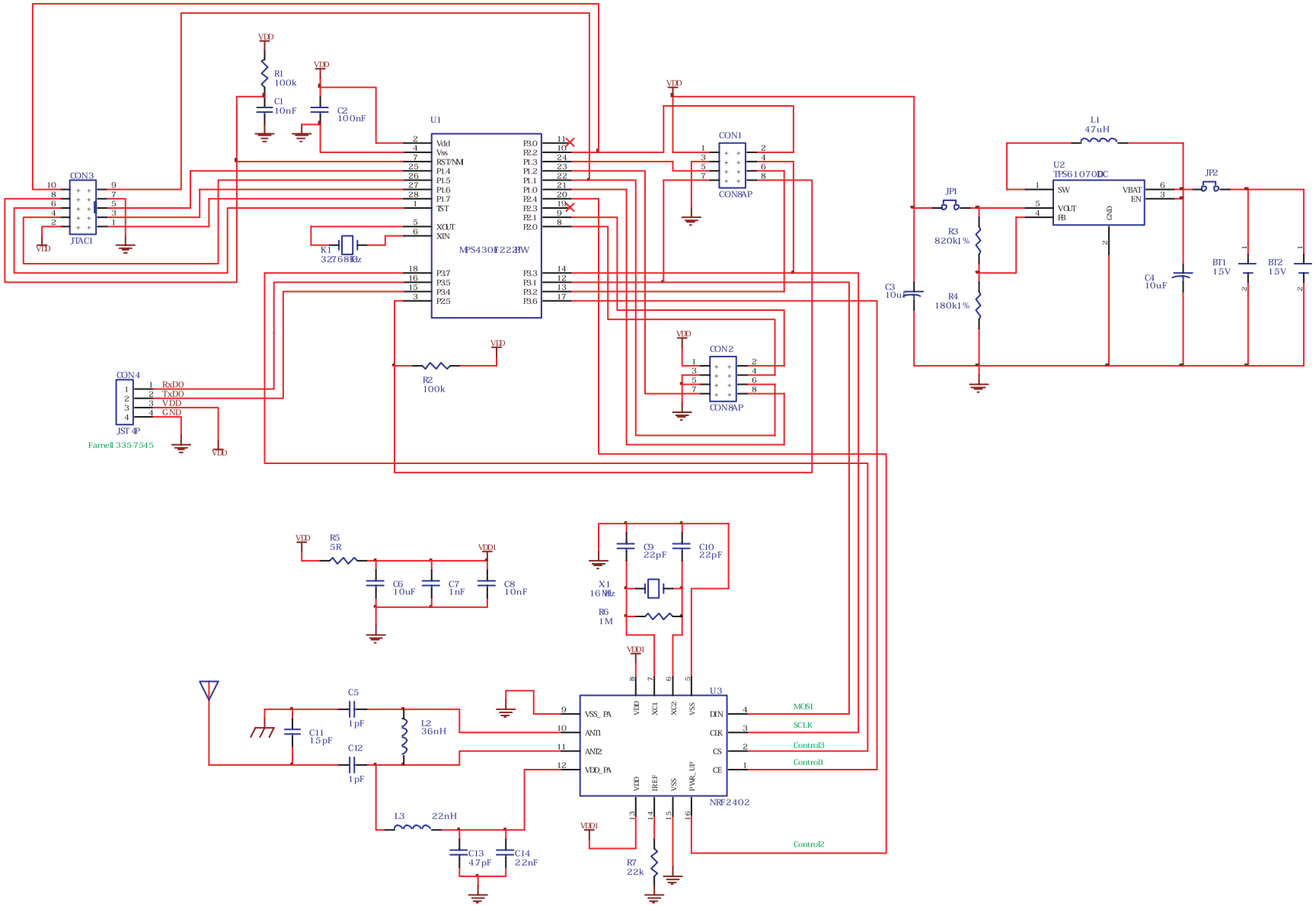


Figure 7b. Schematic Diagram for 3-Button Scroll Wheel Cordless Mouse

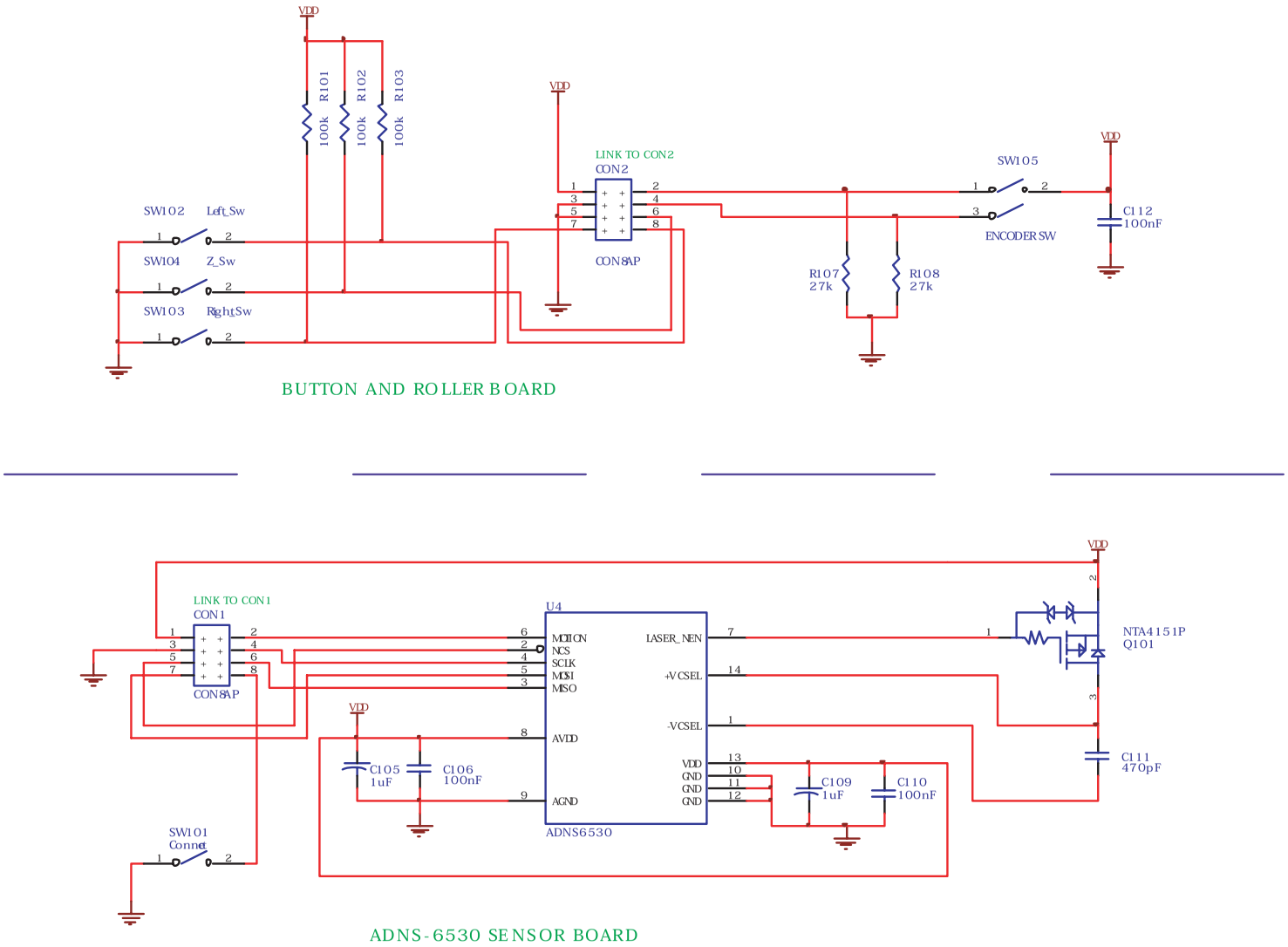


Figure 7c. Schematic Diagram for 3-Button Scroll Wheel Cordless Mouse

Eye Safety

The ADNS-6530 integrated COB LaserStream sensor and the associated components in the schematic of Figure 5 are intended to comply with Class 1 Eye Safety Requirements of IEC 60825-1. Avago Technologies suggests that manufacturers perform testing to verify eye safety on each mouse. It is also recommended to review possible single fault mechanisms beyond those described below in the section "Single Fault Detection". Under normal conditions, the sensor generates the drive current for the VCSEL.

In order to stay below the Class 1 power requirements, LASER_CTRL0 (register 0x1a), LASER_CTRL1 (register 0x1f), LSRPWR_CFG0 (register 0x1c) and LSRPWR_CFG1 (register 0x1d) must be programmed to appropriate values. The ADNS-6530 integrated COB LaserStream sensor which comprised of the sensor and VCSEL; is designed to maintain the output beam power within Class 1 requirements over components manufacturing tolerances and the recommended temperature range when adjusted per the procedure below and implemented as shown in the recommended application circuit of Figure 7. For more information, please refer to Eye Safety Application Note AN5297.

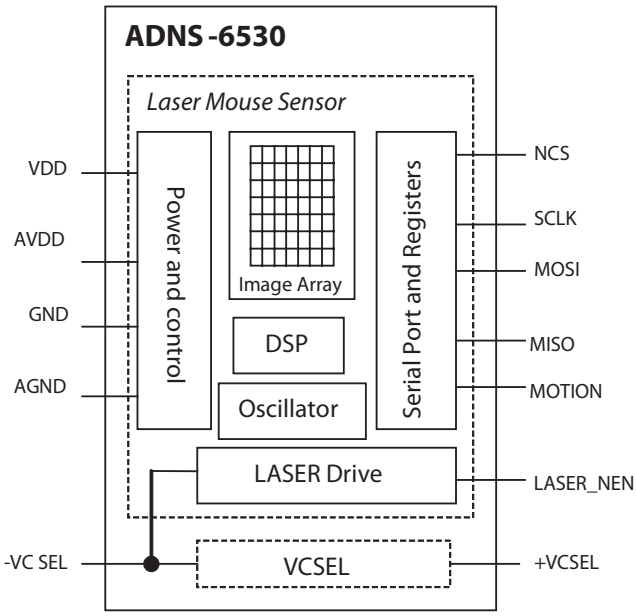


Figure 8. Block diagram of ADNS-6530 integrated COB LaserStream sensor

LASER Drive Mode

The laser is driven in pulsed mode during normal operation. A calibration mode is provided which drives the laser in continuous (CW) operation.

LASER Power Adjustment Procedure

1. The ambient temperature should be 25°C ± 5°C.
2. Set VDD to its permanent value.
3. Set the Range bit (bit 7 of register 0x1a) to 0.
4. Set the Range_C complement bit (bit 7 of register 0x1f) to 1.
5. Enable the Calibration mode by writing to bits [3,2,1] of register 0x1A so the laser will be driven with 100% duty cycle.
6. Write the Calibration mode complement bits to register 0x1f.
7. Set the laser current to the minimum value by writing 0x00 to register 0x1c, and the complementary value 0xFF to register 0x1d.
8. Program registers 0x1c and 0x1d with increasing values to achieve an output power as close to 506uW as possible without exceeding it. If this power is obtained, the calibration is complete, skip to step 12.
9. If it was not possible to achieve the power target, set the laser current to the minimum value by writing 0x00 to register 0x1c, and the complementary value 0xff to register 0x1d.
10. Set the Range and Range_C bits in registers 0x1a and 0x1f, respectively, to choose to the higher laser current range.
11. Program registers 0x1c and 0x1d with increasing values to achieve an output power as close to 506uW as possible without exceeding it.
12. Save the value of registers 0x1a, 0x1c, 0x1d, and 0x1f in non-volatile memory in the mouse. These registers must be restored to these values every time the ADNS-6530 is reset.
13. Reset the mouse, reload the register values from non-volatile memory, enable Calibration mode, and measure the laser power to verify that the calibration is correct.

Good engineering practices such as regular power meter calibration, random quality assurance retest of calibrated mice, etc. should be used to guarantee performance, reliability and safety for the product design.

Parameter	Symbol	Minimum	Maximum	Units	Notes
Laser output power	LOP		716	uW	Class 1 limit with recommended VCSEL and lens.

LASER Output Power

The laser beam output power as measured at the navigation surface plane is specified below. The following conditions apply:

1. The system is adjusted according to the above procedure.
2. The system is operated within the recommended operating temperature range.
3. The VDD value is no greater than 300mV above its value at the time of adjustment.
4. No allowance for optical power meter accuracy is assumed.

Disabling the LASER

LASER_NEN is connected to the gate of a P-channel MOSFET transistor which when ON connects VDD to the LASER. In normal operation, LASER_NEN is low. In the case of a fault condition (ground or VDD at –VCSEL), LASER_NEN goes high to turn the transistor off and disconnect VDD from the LASER.

Single Fault Detection

ADNS-6530 is able to detect a short circuit or fault condition at the –VCSEL pin, which could lead to excessive laser power output. A path to ground on this pin will trigger the fault detection circuit, which will turn off the laser drive current source and set the LASER_NEN output high. When used in combination with external components as shown in the block diagram below, the system will prevent excess laser power for a resistive path to ground at –VCSEL by shutting off the laser. In addition to the ground path fault detection described above, the fault detection circuit is continuously checked for proper operation by internally generating a path to ground with the laser turned off via LASER_NEN. If the –VCSEL pin is shorted to VDD, this test will fail and will be reported as a fault.

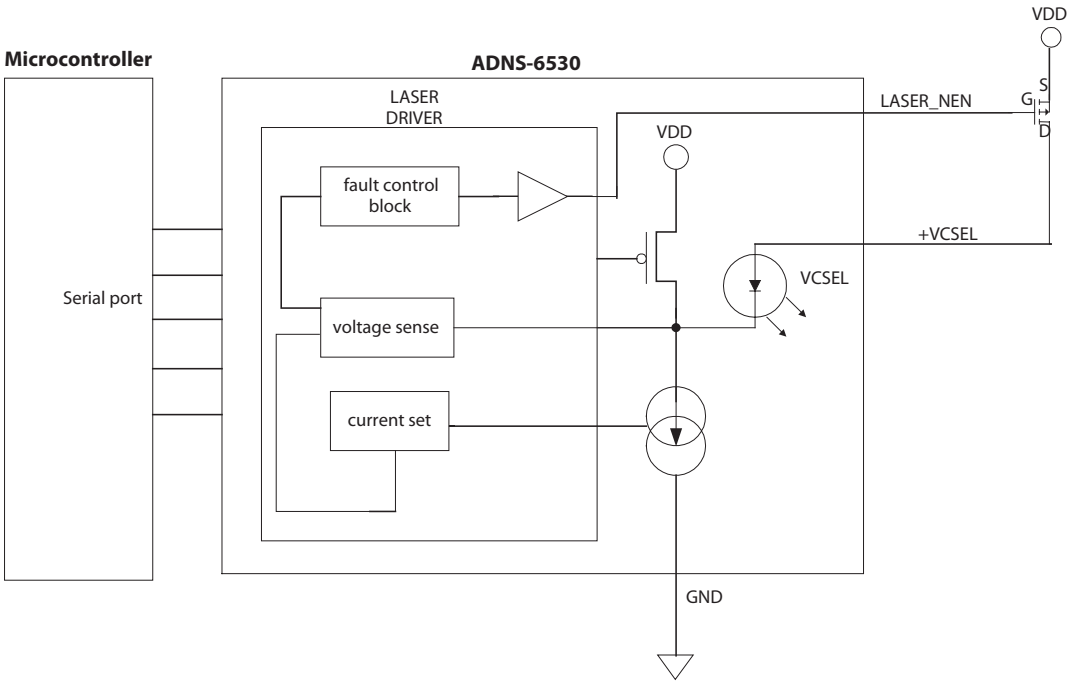


Figure 9. Single Fault Detection and Eye-safety Feature Block Diagram

Regulatory Requirements

- Passes FCC B and worldwide analogous emission limits when assembled into a mouse with shielded cable and following Avago Technologies recommendations.
- Passes IEC-1000-4-3 radiated susceptibility level when assembled into a mouse with shielded cable and following Avago Technologies recommendations.
- Passes EN61000-4-4/IEC801-4 EFT tests when assembled into a mouse with shielded cable and following Avago Technologies recommendations.
- UL flammability level UL94 V-0.
- Provides sufficient ESD creepage/clearance distance to avoid discharge up to 15kV when assembled into a mouse according to usage instructions above.

Absolute Maximum Ratings

VCSEL Die Source Marking	V = A,V	V = C		
Parameter	**Max**	**Max**	**Units**	**Notes**
DC Forward current	12	7.0	mA	
Peak Pulsing current	19	9	mA	Duration = 100ms, 10% duty cycle
Power Dissipation	24	24	mW	
Reverse voltage	5	8	V	I = 10µA
Laser Junction Temperature	150	170	ºC	
Operating case Temperature	5 to 45	5 to 45	ºC	
Storage case Temperature	-40 to +85	-40 to +85	ºC	
Lead Soldering Temperature	260	260	ºC	See reflow profile (Figure 10)
ESD (Human-body model)	2	2	kV	

Comments:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are the stress ratings only and functional operation of the device at these or any other condition beyond those indicated for extended period of time may affect device reliability.
2. The maximum ratings do not reflect eye-safe operation. Eye safe operating conditions are listed in the power adjustment procedure section.
3. The inherent design of this component causes it to be sensitive to electrostatic discharge. The ESD threshold is listed above. To prevent ESD-induced damage, take adequate ESD precautions when handling this product.

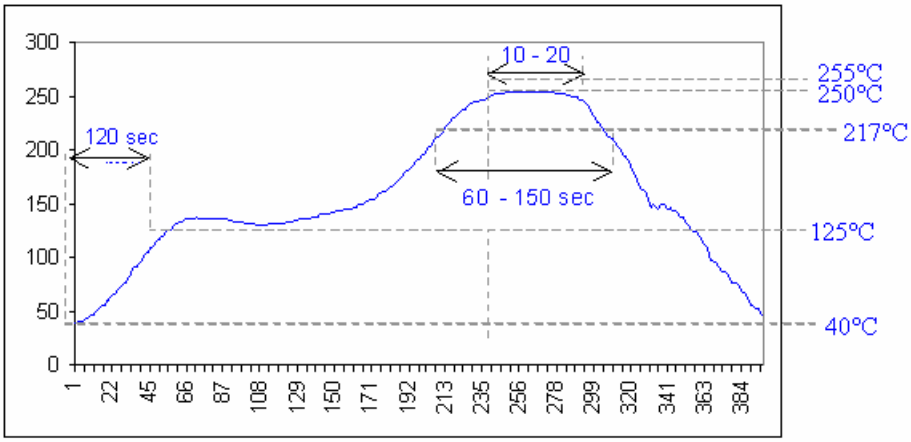


Figure 10. Recommended Soldering Reflow Profile

Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Operating Temperature	T_A	5		40	°C	
Power supply voltage	V_{DD}	2.7	2.8	3.6	Volts	Including noise.
Power supply rise time	V_{RT}	1		100	µsms	0 to 2.8V
Supply noise (Sinusoidal)	V_{NA}			100	mV_{p-p}	10kHz-50MHz
Serial Port Clock Frequency	f_{SCLK}			1	MHz	Active drive, 50% duty cycle
Distance from lens reference plane to surface	Z	2.18	2.40	2.62	mm	Results in +/- 0.22 mm minimum DOF. See Figure 11
Speed	S			20	in/sec	
Acceleration	A			8	g	
Load Capacitance	C_{out}			100	pF	MOTION, MISO
Voltage at -VCSEL	V_{-VCSEL}	0.3		V_{DD}	V	

Optical/Electrical Characteristics (at Tc = 5°C to 45°C):

VCSEL Die Source Marking		V = A,V			V = C				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**	**Notes**
Peak Wavelength	λ	832		865	832		865	nm	
Maximum Radiant Power	LOPmax		4.5			4.0		mW	Maximum output power under any condition. This is not a recommended operating condition and does not meet eye safety requirements.
Wavelength Temperature coefficient	dλ/dT		0.065			0.065		nm/°C	
Wavelength Current coefficient	dλ/dI		0.21			0.3		nm/mA	
Beam Divergence	θFW@1/e^2		15			16		deg	
Threshold current	Ith		4.2			3.0		mA	
Slope Efficiency	SE		0.4			0.35		W/A	
Forward Voltage	VF		2.1	2.4		2.1	2.4	V	At 500uW output power

Comments:

1. VCSELs are sorted into bins as specified in the Figure 7. Package outline drawing (top view). Appropriate binning register data values are used in the application circuit to achieve the target output power. The VCSEL binning is marked on the integrated COB LaserStream sensor package.
2. When driven with current or temperature range greater than specified in the power adjustment procedure section, eye safety limits may be exceeded. The VCSEL should then be treated as a Class 3b laser and as a potential eye hazard.

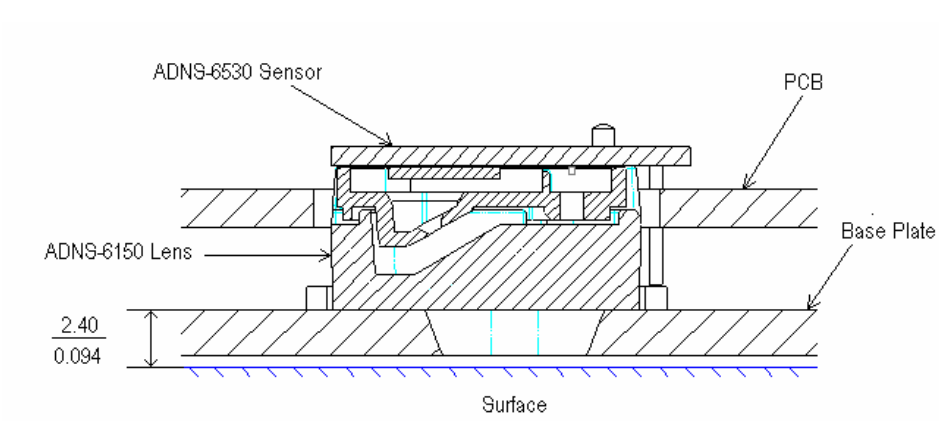


Figure 11. Distance from lens reference plane to surface, Z

AC Electrical Specifications

Electrical Characteristics over recommended operating conditions. Typical values at 25 °C, VDD=2.8V.

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Motion delay after reset	$t_{MOT-RST}$			23	ms	From SW_RESET register write to valid motion, assuming motion is present
Shutdown	t_{STDWN}			50	ms	From Shutdown mode active to low current
Wake from shut-down	t_{WAKEUP}	23			ms	From Shutdown mode inactive to valid motion. Notes: A RESET must be asserted after a shutdown. Refer to section "Notes on Shutdown and Forced Rest", also note $t_{MOT-RST}$
Forced Rest enable	$t_{REST-EN}$			1	s	From RESTEN bits set to low current
Wake from Forced Rest	$t_{REST-DIS}$			1	s	From RESTEN bits cleared to valid motion
MISO rise time	t_{r-MISO}		150	300	ns	C_L = 100pF
MISO fall time	t_{f-MISO}		150	300	ns	C_L = 100pF
MISO delay after SCLK	$t_{DLY-MISO}$			120	ns	From SCLK falling edge to MISO data valid, no load conditions
MISO hold time	$t_{hold-MISO}$	0.5		$1/f_{SCLK}$	us	Data held until next falling SCLK edge
MOSI hold time	$t_{hold-MOSI}$	200			ns	Amount of time data is valid after SCLK rising edge
MOSI setup time	$t_{setup-MOSI}$	120			ns	From data valid to SCLK rising edge
SPI time between write commands	t_{SWW}	30			µs	From rising SCLK for last bit of the first data byte, to rising SCLK for last bit of the second data byte.
SPI time between write and read commands	t_{SWR}	20			µs	From rising SCLK for last bit of the first data byte, to rising SCLK for last bit of the second address byte.
SPI time between read and subsequent commands	$t_{SRW}t_{SRR}$	500			ns	From rising SCLK for last bit of the first data byte, to falling SCLK for the first bit of the address byte of the next command.
SPI read address-data delay	t_{SRAD}	4			µs	From rising SCLK for last bit of the address byte, to falling SCLK for first bit of data being read.
NCS inactive after motion burst	t_{BEXIT}	500			ns	Minimum NCS inactive time after motion burst before next SPI usage
NCS to SCLK active	$t_{NCS-SCLK}$	120			ns	From NCS falling edge to first SCLK rising edge
SCLK to NCS inactive (for read operation)	$t_{SCLK-NCS}$	120			ns	From last SCLK rising edge to NCS rising edge, for valid MISO data transfer
SCLK to NCS inactive (for write operation)	$t_{SCLK-NCS}$	20			us	From last SCLK rising edge to NCS rising edge, for valid MOSI data transfer
NCS to MISO high-Z	$t_{NCS-MISO}$			500	ns	From NCS rising edge to MISO high-Z state
MOTION rise time	$t_{r-MOTION}$		150	300	ns	C_L = 100pF
MOTION fall time	$t_{f-MOTION}$		150	300	ns	C_L = 100pF
Transient Supply Current	I_{DDT}			45	mA	Max supply current during a V_{DD} ramp from 0 to 3.6V

DC Electrical Specifications

Electrical Characteristics over recommended operating conditions. Typical values at 25 °C, VDD=2.8 V.

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
DC Supply Current in various modes	I_{DD_RUN} I_{DD_REST1} I_{DD_REST2} I_{DD_REST3}		4 0.5 0.2 0.06	12 1.8 0.6 0.18	mA	Average current, including LASER current No load on MISO, Motion On black copy surface 500uW laser output power
Peak Supply Current				40	mA	100% LASER current on black copy surface
Shutdown Supply Current	$I_{DDSTDWN}$		1	12	µA	NCS, SCLK = VDDMOSI = GND-MISO = Hi-Z
Input Low Voltage	V_{IL}			0.5	V	SCLK, MOSI, NCS
Input High Voltage	V_{IH}	V_{DD} - 0.5			V	SCLK, MOSI, NCS
Input hysteresis	V_{I_HYS}		100		mV	SCLK, MOSI, NCS
Input leakage current	I_{leak}		±1	±10	µA	Vin = V_{DD}-0.6V, SCLK, MOSI, NCS
Current @ (-VCSEL) pin	I_{LAS}	2		8.5	mA	LOP = 500µW
Output Low Voltage, MISO, LASER_NEN	V_{OL}			0.7	V	Iout= 1mA, MISO, MOTIONIout= 1mA, LASER_NEN
Output High Voltage, MISO, LASER_NEN	V_{OH}	V_{DD} - 0.7			V	Iout= -1mA, MISO, MOTIONIout= -0.5mA, LASER_NEN
Input Capacitance	C_{in}			10	pF	MOSI, NCS, SCLK

Sensor's Typical Performance Characteristics

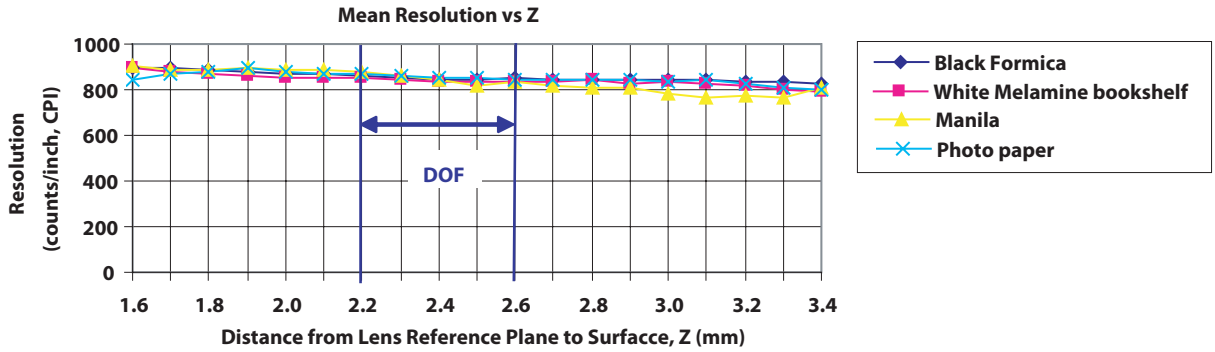


Figure 12. Mean Resolution vs. Z at 800cpi

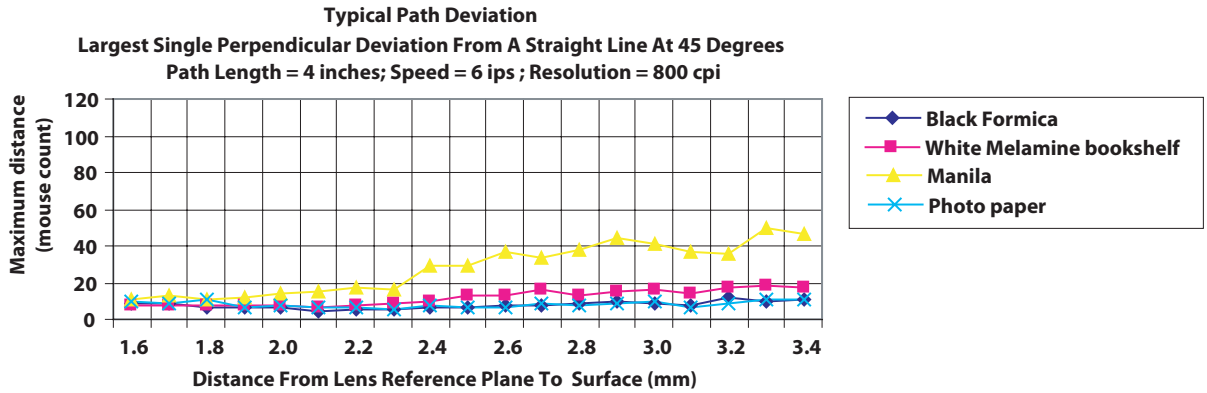


Figure 13. Average Error vs. Distance at 800cpi

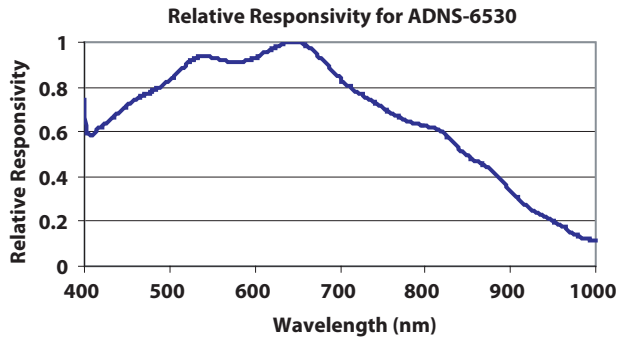


Figure 14. Wavelength Responsivity

VCSEL's Typical Characteristics

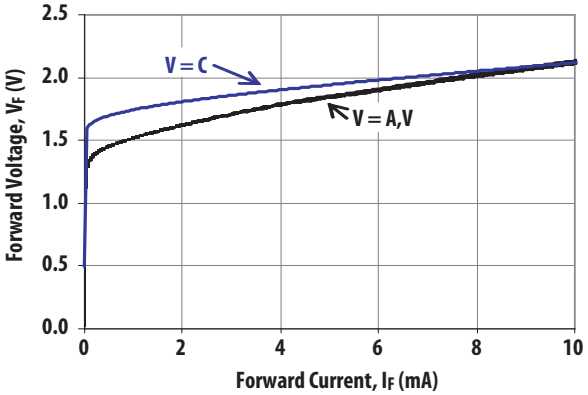


Figure 15. Forward Voltage vs. Forward Current for VCSEL

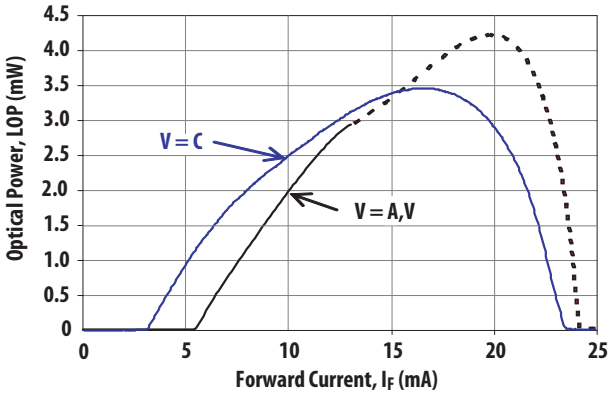


Figure 16. Optical Power vs. Forward Current for VCSEL

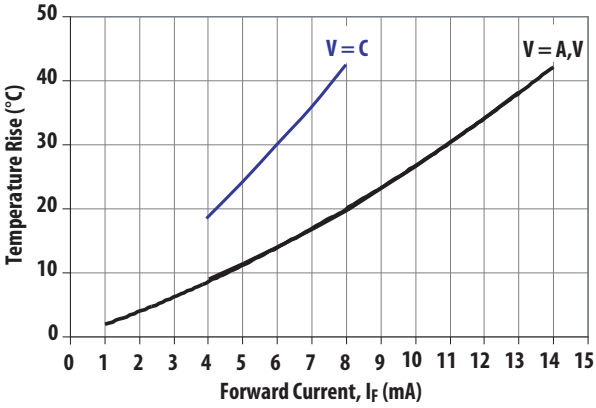


Figure 17. Junction Temperature Rise vs. Forward Current for VCSEL

Power management modes

The ADNS-6530 has three power-saving modes. Each mode has a different motion detection period, affecting response time to mouse motion (Response Time). The sensor automatically changes to the appropriate mode, depending on the time since the last reported motion (Downshift Time). The parameters of each mode are shown in the following table.

Mode	Response Time (nominal)	Downshift Time (nominal)
Rest 1	16.5ms	237ms
Rest 2	82ms	8.4s
Rest 3	410ms	504s

Motion Pin Timing

The motion pin is a level-sensitive output that signals the micro-controller when motion has occurred. The motion pin is lowered whenever the motion bit is set; in other words, whenever there is data in the Delta_X or Delta_Y registers. Clearing the motion bit (by reading Delta_X and Delta_Y, or writing to the Motion register) will put the motion pin high.

LASER Mode

For power savings, the VCSEL will not be continuously on. ADNS-6530 will flash the VCSEL only when needed.

Synchronous Serial Port

The synchronous serial port is used to set and read parameters in the ADNS-6530, and to read out the motion information. The port is a four-wire port. The host micro-controller always initiates communication; the ADNS-6530 never initiates data transfers. SCLK, MOSI, and NCS may be driven directly by a micro-controller. The port pins may be shared with other SPI slave devices. When the NCS pin is high, the inputs are ignored and the output is tri-stated.

The lines that comprise the SPI port:

SCLK: Clock input. It is always generated by the master (the micro-controller).

MOSI: Input data. (Master Out/Slave In)

MISO: Output data. (Master In/Slave Out)

NCS: Chip select input (active low). NCS needs to be low to activate the serial port; otherwise, MISO will be high Z, and MOSI & SCLK will be ignored. NCS can also be used to reset the serial port in case of an error.

Chip Select Operation

The serial port is activated after NCS goes low. If NCS is raised during a transaction, the entire transaction is aborted and the serial port will be reset. This is true for all transactions. After a transaction is aborted, the normal address-to-data or transaction-to-transaction delay is still required before beginning the next transaction. To improve communication reliability, all serial transactions should be framed by NCS. In other words, the port should not remain enabled during periods of non-use because ESD and EFT/B events could be interpreted as serial communication and put the chip into an unknown state. In addition, NCS must be raised after each burst-mode transaction is complete to terminate burst-mode. The port is not available for further use until burst-mode is terminated.

Write Operation

Write operation, defined as data going from the micro-controller to the ADNS-6530, is always initiated by the micro-controller and consists of two bytes. The first byte contains the address (seven bits) and has a "1" as its MSB to indicate data direction. The second byte contains the data. The ADNS-6530 reads MOSI on rising edges of SCLK.

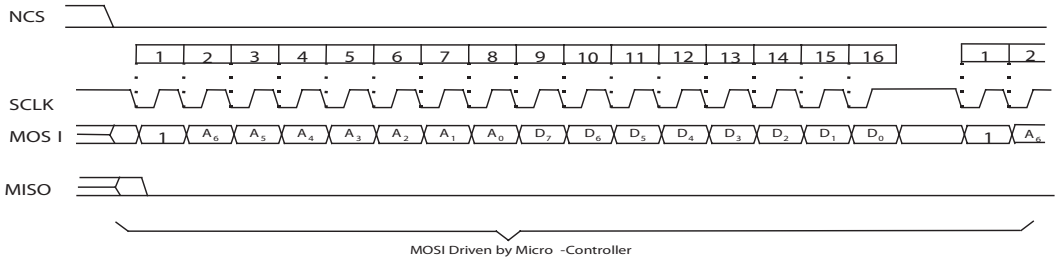


Figure 18. Write Operation

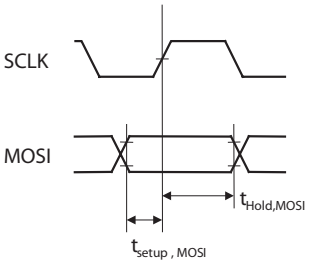


Figure 19. MOSI Setup and Hold Time

Read Operation

A read operation, defined as data going from the ADNS-6530 to the micro-controller, is always initiated by the micro-controller and consists of two bytes. The first byte contains the address, is sent by the micro-controller over MOSI, and has a "0" as its MSB to indicate data direction. The second byte contains the data and is driven by the ADNS-6530 over MISO. The sensor outputs MISO bits on falling edges of SCLK and samples MOSI bits on every rising edge of SCLK.

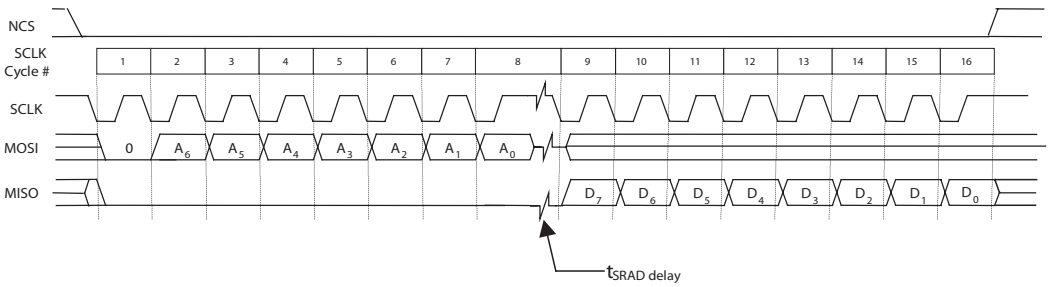


Figure 20. Read Operation

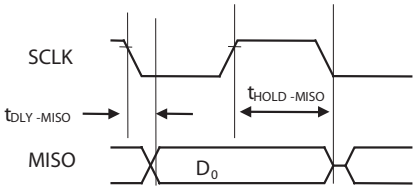


Figure 21. MISO Delay and Hold Time

Note: The 0.5/fSCLK minimums high state of SCLK is also the minimum MISO data hold time of the ADNS-6530. Since the falling edge of SCLK is actually the start of the next read or write command, the ADNS-6530 will hold the state of data on MISO until the falling edge of SCLK.

Required timing between Read and Write Commands

There are minimum timing requirements between read and write commands on the serial port.

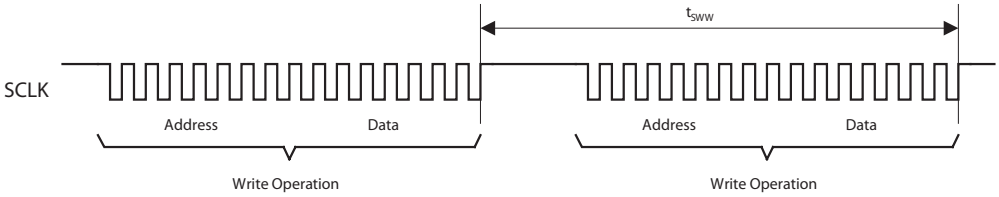


Figure 22. Timing between two write commands

If the rising edge of the SCLK for the last data bit of the second write command occurs before the required delay (t_{SWW}), then the first write command may not complete correctly.

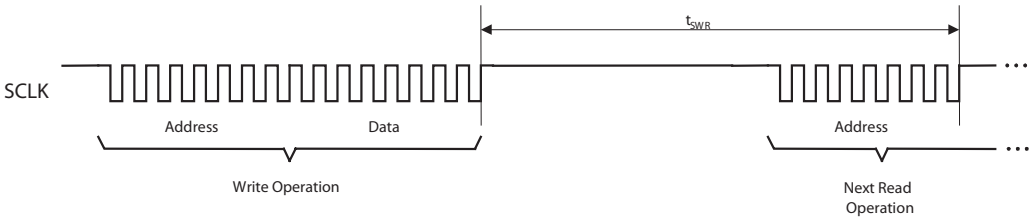


Figure 23. Timing between write and read commands

If the rising edge of SCLK for the last address bit of the read command occurs before the required delay (t_{SWR}), the write command may not complete correctly.

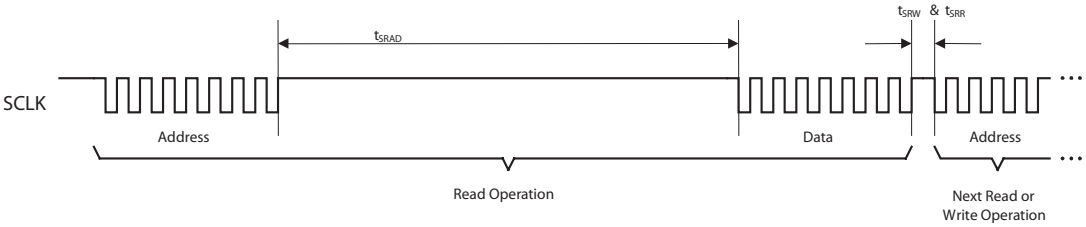


Figure 24. Timing between read and either write or subsequent read commands

During a read operation SCLK should be delayed at least t_{SRAD} after the last address data bit to ensure that the ADNS-6530 has time to prepare the requested data. The falling edge of SCLK for the first address bit of either the read or write command must be at least t_{SRR} or t_{SRW} after the last SCLK rising edge of the last data bit of the previous read operation.

Burst Mode Operation

Burst mode is a special serial port operation mode that may be used to reduce the serial transaction time for a motion read. The speed improvement is achieved by continuous data clocking to or from multiple registers without the need to specify the register address, and by not requiring the normal delay period between data bytes.

Burst mode is activated by reading the Motion_Burst register. The ADNS-6530 will respond with the contents of the Motion, Delta_X, Delta_Y, SQUAL, Shutter_Upper, Shutter_Lower and Maximum_Pixel registers in that order. The burst transaction can be terminated anywhere in the sequence after the Delta_X value by bringing the NCS pin high. After sending the register address, the micro-controller must wait t_{SRAD} and then begin reading data. All data bits can be read with no delay between bytes by driving SCLK at the normal rate. The data are latched into the output buffer after the last address bit is received. After the burst transmission is complete, the micro-controller must raise the NCS line for at least t_{BEXIT} to terminate burst mode. The serial port is not available for use until it is reset with NCS, even for a second burst transmission.

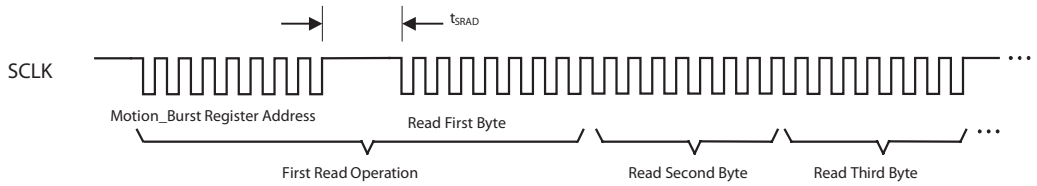


Figure 25. Motion Burst Timing

Notes on Power-up

The ADNS-6530 does not perform an internal power up self-reset; the POWER_UP_RESET register must be written every time power is applied. The appropriate sequence is as follows:

1. Apply power
2. Drive NCS high, then low to reset the SPI port
3. Write 0x5a to register 0x3a
4. Wait for t_{WAKEUP}
5. Write 0xFE to register 0x28
6. Read from registers 0x02, 0x03 and 0x04 (or read these same 3 bytes from burst motion register 0x42) one time regardless of the motion pin state.

During power-up there will be a period of time after the power supply is high but before any clocks are available. The table below shows the state of the various pins during power-up and reset.

State of Signal Pins After VDD is Valid

Pin	On Power-Up	NCS High before Reset	NCS Low before Reset	After Reset
NCS	Functional	High	Low	Functional
MISO	Undefined	Undefined	Functional	Depends on NCS
SCLK	Ignored	Ignored	Functional	Depends on NCS
MOSI	Ignored	Ignored	Functional	Depends on NCS
-VCSEL	Undefined	Undefined	Undefined	Functional
MOTION	Undefined	Undefined	Undefined	Functional
LASER_NEN	Undefined	Undefined	Undefined	Functional

Notes on Shutdown and Forced Rest

The ADNS-6530 can be set in Rest mode through the Configuration_Bits register (0x11). This is to allow for further power savings in applications where the sensor does not need to operate all the time.

The ADNS-6530 can be set in Shutdown mode by writing 0xe7 to register 0x3b. The SPI port should not be accessed when Shutdown mode is asserted, except the power-up command (writing 0x5a to register 0x3a). (Other ICs on the same SPI bus can be accessed, as long as the sensor's NCS pin is not asserted.) The table below shows the state of various pins during shutdown. To deassert Shutdown mode:

1. Write 0x5a to register 0x3a
2. Wait for t_{WAKEUP}
3. Write 0xFE to register 0x28
4. Any register settings must then be reloaded.

Pin	Status when Shutdown Mode
NCS	Functional *1
MISO	Undefined *2
SCLK	Ignore if NCS = 1 *3
MOSI	Ignore if NCS = 1 *4
XYLASER	High (off)
LASER_NEN	High (off)
MOTION	Undefined *2

*1 NCS pin must be held to 1 (high) if SPI bus is shared with other devices. It is recommended to hold to 1 (high) during Power Down unless powering up the Sensor. It must be held to 0 (low) if the sensor is to be re-powered up from shutdown (writing 0x5a to register 0x3a).

*2 Depends on last state

*3 SCLK is ignored if NCS is 1 (high). It is functional if NCS is 0 (low).

*4 MOSI is ignored if NCS is 1 (high). If NCS is 0 (low), any command present on the MOSI pin will be ignored except power-up command (writing 0x5a to register 0x3a).

Note: There are long wakeup times from shutdown and forced Rest. These features should not be used for power management during normal mouse motion.

Registers

The ADNS-6530 registers are accessible via the serial port. The registers are used to read motion data and status as well as to set the device configuration.

Address	Register	Read/Write	Default Value
0x00	Product_ID	R	0x20
0x01	Revision_ID	R	0x03
0x02	Motion	R/W	0x00
0x03	Delta_X	R	0x00
0x04	Delta_Y	R	0x00
0x05	SQUAL	R	0x00
0x06	Shutter_Upper	R	0x00
0x07	Shutter_Lower	R	0x64
0x08	Maximum_Pixel	R	0xd0
0x09	Pixel_Sum	R	0x80
0x0a	Minimum_Pixel	R	0x00
0x0b	Pixel_Grab	R/W	0x00
0x0c	CRC0	R	0x00
0x0d	CRC1	R	0x00
0x0e	CRC2	R	0x00
0x0f	CRC3	R	0x00
0x10	Self_Test	W	NA
0x11	Configuration_Bits	R/W	0x03
0x12-0x19	Reserved		
0x1a	LASER_CTRL0	R/W	0x00
0x1d	LSRPWR_CFG1	R/W	0x00
0x1e	Reserved		
0x1f	LASER_CTRL1	R/W	0x01
0x20-0x2d	Reserved		
0x2e	Observation	R/W	0x00
0x2f-0x39	Reserved		
0x3a	POWER_UP_RESET	W	NA
0x3b	Shutdown	W	NA
0x3c-0x3d	Reserved		
0x3e	Inverse_Revision_ID	R	0xfc
0x3f	Inverse_Product_ID	R	0xdf
0x42	Motion_Burst	R	0x00

Product_ID **Address: 0x00**

Access: Read Reset Value: 0x20

Bit	7	6	5	4	3	2	1	0
Field	PID_7	PID_6	PID_5	PID_4	PID_3	PID_2	PID_1	PID_0

Data Type : 8-Bit unsigned integer

USAGE : This register contains a unique identification assigned to the ADNS-6530. The value in this register does not change; it can be used to verify that the serial communications link is functional.

Revision_ID **Address: 0x01**

Access: Read Reset Value: 0x03

Bit	7	6	5	4	3	2	1	0
Field	RID_7	RID_6	RID_5	RID_4	RID_3	RID_2	RID_1	RID_0

Data Type : 8-Bit unsigned integer

USAGE : This register contains the IC revision. It is subject to change when new IC versions are released.

Motion	**Address: 0x02**
Access: Read/Write	Reset Value: 0x00

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	MOT	PIXRDY	PIXFIRST	OVF	LP_VALID	FAULT	Reserved	Reserved

Data Type : Bit field.

USAGE : Register 0x02 allows the user to determine if motion has occurred since the last time it was read. If the MOT bit is set, then the user should read registers 0x03 and 0x04 to get the accumulated motion. Read this register before reading the Delta_X and Delta_Y registers.

Writing anything to this register clears the MOT and OVF bits, Delta_X and Delta_Y registers. The written data byte is not saved.

Internal buffers can accumulate more than eight bits of motion for X or Y. If one of the internal buffers overflows, then absolute path data is lost and the OVF bit is set. To clear the overflow, write anything to this register.

Check the OVF bit if more than 4" of motion is accumulated without reading it. If bit set, discard the motion as erroneous. Write anything to this register to clear the overflow condition.

The PIXRDY bit will be set whenever a valid pixel data byte is available in the Pixel_Dump register. Check that this bit is set before reading from Pixel_Dump. To ensure that the Pixel_Grab pointer has been reset to pixel 0,0 on the initial write to Pixel_Grab, check to see if PIXFIRST is set to high.

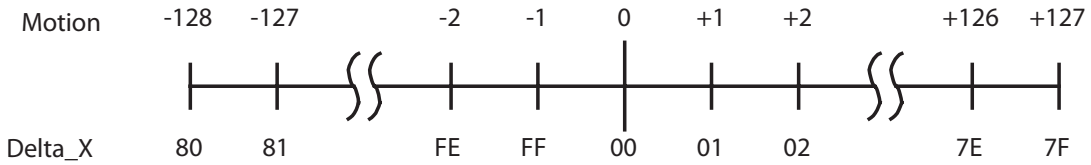
Field Name	**Description**
MOT	Motion since last report **0 = no motion** 1 = motion occurred, data ready for reading in Delta_X and Delta_Y registers
PIXRDY	Pixel Dump data byte is available in Pixel_Dump register **0 = data not available** 1 = data available
PIXFIRST	This bit is set when the Pixel_Grab register is written to or when a complete pixel array has been read, initiating an increment to pixel 0,0. **0 = Pixel_Grab data not from pixel 0,0** 1 = Pixel_Grab data is from pixel 0,0
OVF	Motion overflow, ΔY and/or ΔX buffer has overflowed since last report **0 = no overflow** 1 = overflow has occurred
LP_VALID	Laser Power Settings **0 = register 0x1a and register 0x1f or register 0x1c and register 0x1d do not have complementary values** 1 = laser power is valid
FAULT	Indicates that -VCSEL is shorted to GND or VDD **0 = no fault detected** 1 = fault detected

Note: Avago Technologies recommends that registers 0x02, 0x03 and 0x04 be read sequentially.

Delta_X			**Address: 0x03**					
Access: Read			Reset Value: 0x00					
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0

Data Type : 8-bit 2's complement number.

USAGE : X movement is counts since last report. Absolute value is determined by resolution. Reading clears the register.

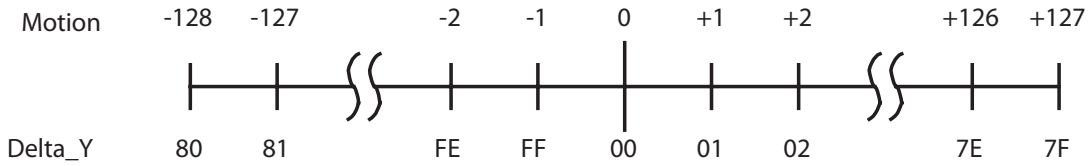


Note: Avago Technologies recommends that registers 0x02, 0x03 and 0x04 be read sequentially.

Delta_Y			**Address: 0x04**					
Access: Read			Reset Value: 0x00					
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0

Data Type : Eight bit 2's complement number.

USAGE : Y movement is counts since last report. Absolute value is determined by resolution. Reading clears the register.



Note: Avago Technologies recommends that registers 0x02, 0x03 and 0x04 be read sequentially.

SQUAL			**Address: 0x05**					
Access: Read			Reset Value: 0x00					
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	SQ_7	SQ_6	SQ_5	SQ_4	SQ_3	SQ_2	SQ_1	SQ_0

Data Type : Upper 8 bits of a 9-bit unsigned integer.

USAGE : SQUAL (Surface Quality) is a measure of the number of valid features visible by the sensor in the current frame.

The maximum SQUAL register value is 162. Since small changes in the current frame can result in changes in SQUAL, variations in SQUAL when looking at a surface are expected. The graph below shows 800 sequentially acquired SQUAL values, while a sensor was moved slowly over white paper. SQUAL is nearly equal to zero, if there is no surface below the sensor. SQUAL is typically maximized when the navigation surface is at the optimum distance from the imaging lens (the nominal Z-height).

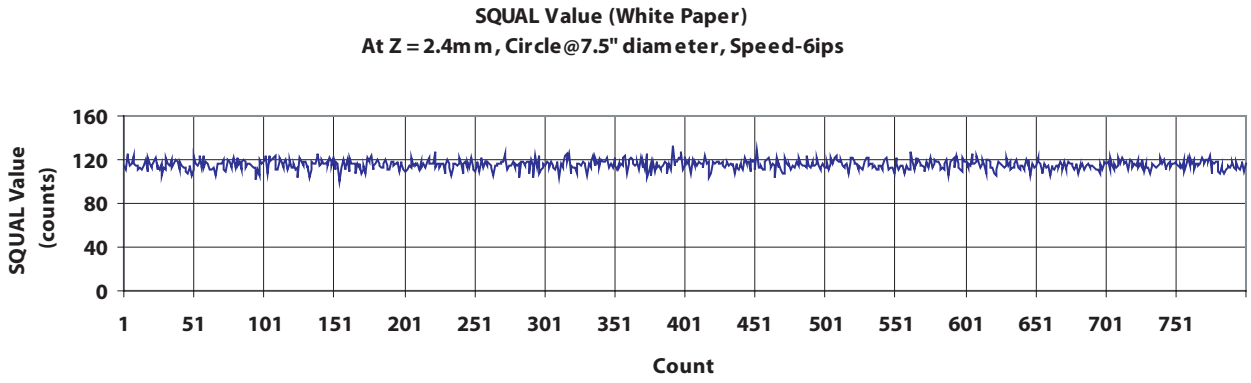


Figure 26. SQUAL Values at 800cpi (White Paper)

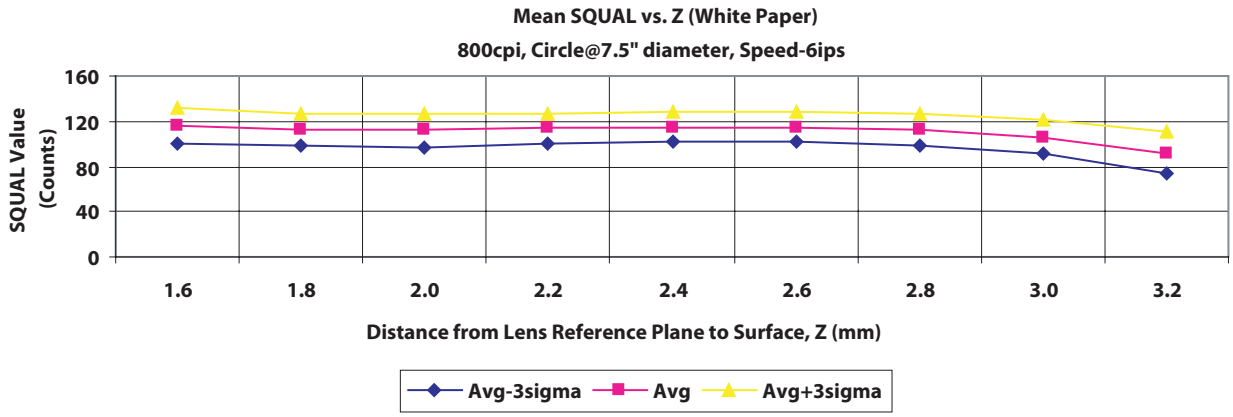


Figure 27. Mean SQUAL vs. Z (White Paper)

Shutter_Upper			**Address: 0x06**					
Access: Read			Reset Value: 0x00					
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	S_{15}	S_{14}	S_{13}	S_{12}	S_{11}	S_{10}	S_9	S_8

Shutter_Lower			**Address: 0x07**					
Access: Read			Reset Value: 0x64					
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	S_7	S_6	S_5	S_4	S_3	S_2	S_1	S_0

Data Type : Sixteen bit unsigned integer.

USAGE : Units are clock cycles. Read Shutter_Upper first, then Shutter_Lower. They should be read consecutively. The shutter is adjusted to keep the average and maximum pixel values within normal operating ranges. The shutter value is automatically adjusted.

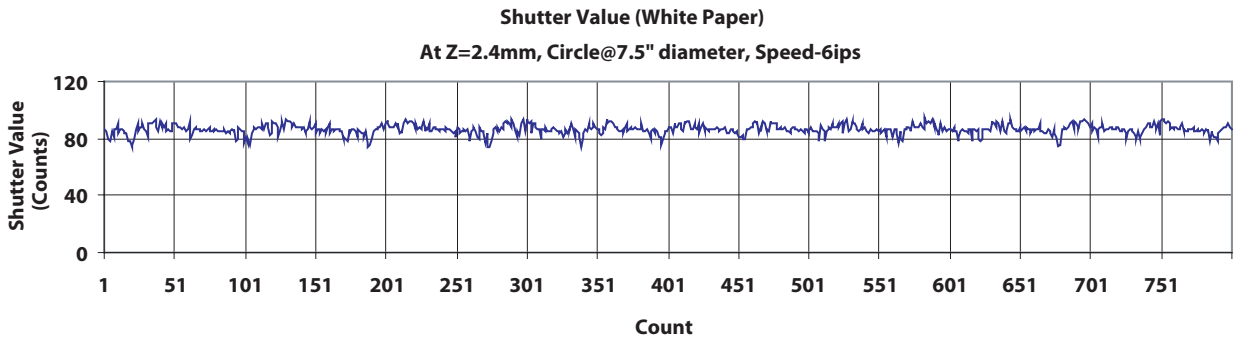


Figure 28. Shutter Values at 800cpi (White Paper)

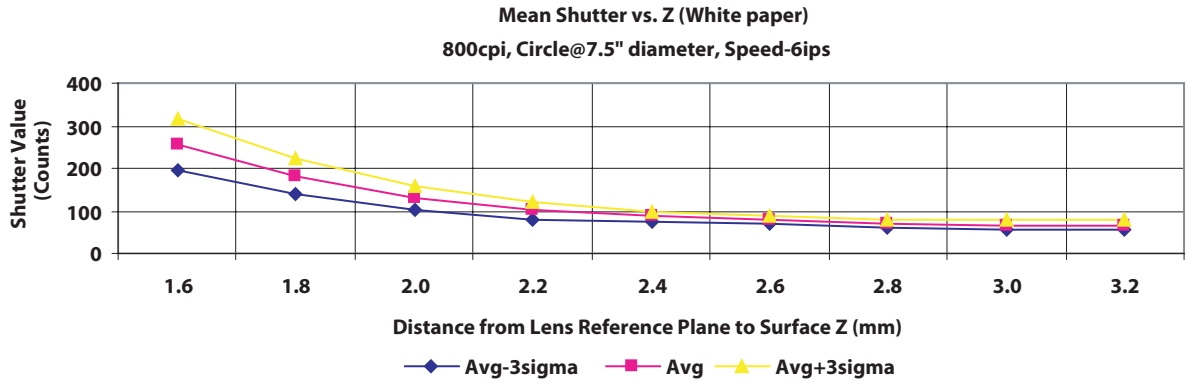


Figure 29. Mean Shutter vs. Z (White Paper)

Maximum_Pixel **Address: 0x08**

Access: Read Reset Value: 0xd0

Bit	7	6	5	4	3	2	1	0
Field	MP_7	MP_6	MP_5	MP_4	MP_3	MP_2	MP_1	MP_0

Data Type : Eight-bit number.

USAGE : Maximum Pixel value in current frame. Minimum value = 0, maximum value = 254. The maximum pixel value can vary with every frame.

Pixel_Sum **Address: 0x09**

Access: Read Reset Value: 0x80

Bit	7	6	5	4	3	2	1	0
Field	AP_7	AP_6	AP_5	AP_4	AP_3	AP_2	AP_1	AP_0

Data Type : High 8 bits of an unsigned 17-bit integer.

USAGE : This register is used to find the average pixel value. It reports the upper eight bits of a 17-bit counter, which sums all pixels in the current frame. It may be described as the full sum divided by 512. To find the average pixel value, use the following formula:

Average Pixel = Register Value * 512/484 = Register Value * 1.058

The maximum register value is 241. The minimum is 0.
The pixel sum value can change on every frame.

Minimum_Pixel **Address: 0x0a**

Access: Read Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	MP_7	MP_6	MP_5	MP_4	MP_3	MP_2	MP_1	MP_0

Data Type : Eight-bit number.

USAGE : Minimum Pixel value in current frame. Minimum value = 0, maximum value = 254. The minimum pixel value can vary with every frame.

Pixel_Grab			**Address: 0x0b**					
Access: Read/Write			Reset Value: 0x00					
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	PD_7	PD_6	PD_5	PD_4	PD_3	PD_2	PD_1	PD_0

Data Type : Eight-bit word.

USAGE : For test purposes, the sensor will read out the contents of the pixel array, one pixel per frame. To start a pixel grab, write anything to this register to reset the pointer to pixel 0,0. Then read the PIXRDY bit in the Motion register. When the PIXRDY bit is set, there is valid data in this register to read out. After the data in this register is read, the pointer will automatically increment to the next pixel. Reading may continue indefinitely; once a complete frame's worth of pixels has been read, PIXFIRST will be set to high to indicate the start of the first pixel and the address pointer will start at the beginning location again.

First Pixel

0	22	44	66	88	110	132	154	176	198	220	242	264	286	308	330	352	374	396	418	440	462
1	23	45	67	89	111	133	155	177	199	221	243	265	287	309	331	353	375	397	419	441	463
2	24	46	68	90	112	134	156	178	200	222	244	266	288	310	332	354	376	398	420	442	464
3	25	47	69	91	113	135	157	179	201	223	245	267	289	311	333	355	377	399	421	443	465
4	26	48	70	92	114	136	158	180	202	224	246	268	290	312	334	356	378	400	422	444	466
5	27	49	71	93	115	137	159	181	203	225	247	269	291	313	335	357	379	401	423	445	467
6	28	50	72	94	116	138	160	182	204	226	248	270	292	314	336	358	380	402	424	446	468
7	29	51	73	95	117	139	161	183	205	227	249	271	293	315	337	359	381	403	425	447	469
8	30	52	74	96	118	140	162	184	206	228	250	272	294	316	338	360	382	404	426	448	470
9	31	53	75	97	119	141	163	185	207	229	251	273	295	317	339	361	383	405	427	449	471
10	32	54	76	98	120	142	164	186	208	230	252	274	296	318	340	362	384	406	428	450	472
11	33	55	77	99	121	143	165	187	209	231	253	275	297	319	341	363	385	407	429	451	473
12	34	56	78	100	122	144	166	188	210	232	254	276	298	320	342	364	386	408	430	452	474
13	35	57	79	101	123	145	167	189	211	233	255	277	299	321	343	365	387	409	431	453	475
14	36	58	80	102	124	146	168	190	212	234	256	278	300	322	344	366	388	410	432	454	476
15	37	59	81	103	125	147	169	191	213	235	257	279	301	323	345	367	389	411	433	455	477
16	38	60	82	104	126	148	170	192	214	236	258	280	302	324	346	368	390	412	434	456	478
17	39	61	83	105	127	149	171	193	215	237	259	281	303	325	347	369	391	413	435	457	479
18	40	62	84	106	128	150	172	194	216	238	260	282	304	326	348	370	392	414	436	458	480
19	41	63	85	107	129	151	173	195	217	239	261	283	305	327	349	371	393	415	437	459	481
20	42	64	86	108	130	152	174	196	218	240	262	284	306	328	350	372	394	416	438	460	482
21	43	65	87	109	131	153	175	197	219	241	263	285	307	329	351	373	395	417	439	461	483

Last Pixel

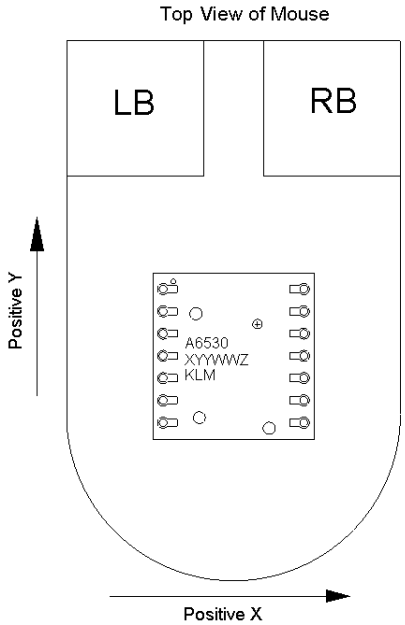


Figure 30. Pixel Address Map (Sensor looking on the navigation surface through the ADNS-6150 Lens)

CRC0 **Address: 0x0c**

Access: Read Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	$CRC0_7$	$CRC0_6$	$CRC0_5$	$CRC0_4$	$CRC0_3$	$CRC0_2$	$CRC0_1$	$CRC0_0$

Data Type : Eight-bit number

USAGE : Register 0x0c reports the first byte of the system self test results. Value = 9C.

CRC1 **Address: 0x0d**

Access: Read Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	$CRC1_7$	$CRC1_6$	$CRC1_5$	$CRC1_4$	$CRC1_3$	$CRC1_2$	$CRC1_1$	$CRC1_0$

Data Type : Eight bit number

USAGE : Register 0x0c reports the second byte of the system self test results. Value = F6.

CRC2 **Address: 0x0e**

Access: Read Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	$CRC2_7$	$CRC2_6$	$CRC2_5$	$CRC2_4$	$CRC2_3$	$CRC2_2$	$CRC2_1$	$CRC2_0$

Data Type : Eight-bit number

USAGE : Register 0x0e reports the third byte of the system self test results. Value = 01.

CRC3 **Address: 0x0f**

Access: Read Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	$CRC3_7$	$CRC3_6$	$CRC3_5$	$CRC3_4$	$CRC3_3$	$CRC3_2$	$CRC3_1$	$CRC3_0$

Data Type : Eight-bit number

USAGE : Register 0x0f reports the fourth byte of the system self test results. Value = 78.

Self_Test **Address: 0x10**

Access: Write Reset Value: NA

Bit	7	6	5	4	3	2	1	0
Field	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	TESTEN

Data Type : Bit field

USAGE : Set the TESTEN bit in register 0x10 to start the system self-test. The test takes 250ms. During this time, do not write or read through the SPI port. Results are available in the CRC0-3 registers. After self-test, reset the chip to start normal operation.

Field Name	Description
TESTEN	Enable System Self Test **0=Disable** 1=Enable

Configuration_bits **Address: 0x11**

Access: Read/Write Reset Value: 0x03

Bit	7	6	5	4	3	2	1	0
Field	RES	Reserved	$RESTEN_1$	$RESTEN_0$	Reserved	Reserved	Reserved	Reserved

Data Type : Bit field

USAGE : Register 0x11 allows the user to change the configuration of the sensor. Setting the RESTEN1-0 bits forces the sensor into Rest mode, as described in the power modes section above. The RES bit allows selection between 400 and 800cpi resolution.

Note: Forced Rest has a long wakeup time and should not be used for power management during normal mouse motion.

Field Name	Description
$RESTEN_{1-0}$	Puts chip into Rest mode **00 = normal operation** 01 = force Rest1 11 = force Rest3
RES	Sets resolution **0 = 400** 1 = 800

Reserved **Address: 0x12-0x19**

LASER_CTRL0 **Address: 0x1a**

Access: Read/Write Reset Value: 0x00

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	Range	Reserved	0	Reserved	CAL_2	CAL_1	CAL_0	Force_Disable

Data Type : Bit field

USAGE : This register is used to control the laser drive. Bits 5 and 7 require complement values in register 0x1F. If the registers do not contain complementary values for these bits, the laser is turned off and the LP_VALID bit in the MOTION register is set to 0. The registers may be written in any order after the power ON reset.

Field Name	**Description**
Range	Rbin Settings **0 = Laser current range from approximately 2mA to 7mA** 1 = Laser current range from approximately 5mA to 13mA
Bit 5	Must be always set to 0
CAL_{2-0}	Laser calibration mode - Write 101b to bits [3,2,1] to set the laser to continuos ON (CW) mode. - Write 000b to exit laser calibration mode, all other values are not recommended. Reading the Motion register (0x03 or 0x42) will reset the value to 000b and exit calibration mode
Force_Disable	LASER force diable **0 = LASER_NEN functions as normal** 1 = LASER_NEN output is high

Reserved **Address: 0x1b**

LSRPWR_CFG0 **Address: 0x1c**

Access: Read and Write Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	LP_7	LP_6	LP_5	LP_4	LP_3	LP_2	LP_1	LP_0

Data Type : 8-Bit unsigned

USAGE : This register is used to set the laser current. It is to be used together with register 0x1D, where register 0x1D contains the complement of register 0x1C. If the registers do not contain complementary values, the laser is turned off and the LP_VALID bit in the MOTION register is set to 0. The registers may be written in any order after the power ON reset.

Field Name	Description
LP_7 - LP_0	Controls the 8-bit DAC for adjusting laser current. One step is equivalent to (1/384)*100% = 0.26% drop of relative laser current. Refer to the table below for examples of relative laser current settings.

LP_7 - LP_3	LP_2	LP_1	LP_0	Relative Laser Current
00000	**0**	**0**	**0**	**33.59%**
00000	0	0	1	33.85%
00000	0	1	0	34.11%
: :	:	:	:	: :
11111	1	0	1	99.48%
11111	1	1	0	99.74%
11111	1	1	1	100%

LSRPWR_CFG1 **Address: 0x1d**

Access: Read and Write Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	LPC_7	LPC_6	LPC_5	LPC_4	LPC_3	LPC_2	LPC_1	LPC_0

Data Type : 8-Bit unsigned

USAGE : The value in this register must be a complement of register 0x1C for laser current to be as programmed, otherwise the laser is turned off and the LP_VALID bit in the MOTION register is set to 0. Registers 0x1C and 0x1D may be written in any order after power ON reset.

Reserved **Address: 0x1e**

LASER_CTRL1 **Address: 0x1f**

Access: Read and Write Reset Value: 0x01

Bit	7	6	5	4	3	2	1	0
Field	Range_C	Reserved	1	Reserved	Reserved	Reserved	Reserved	Reserved

Data Type : 8-Bit unsigned

USAGE : Bits 5 and 7 of this register must be the complement of the corresponding bits in register 0x1A for the VCSEL control to be as programmed, otherwise the laser turned is off and the LP_VALID bit in the MOTION register is set to 0. Registers 0x1A and 0x1F may be written in any order after power ON reset.

Field Name	Description
Range-C	Complementary value of Bit-7 in register 0x1a
Bit-5	Must be always set to 1

Reserved **Address: 0x20-0x2d**

Observation **Address: 0x2e**

Access: Read/Write Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	$MODE_1$	$MODE_0$	Reserved	OBS_4	OBS_3	OBS_2	OBS_1	OBS_0

Data Type : Bit field

USAGE : Register 0x2e provides bits that are set every frame. It can be used during EFT/B testing to check that the chip is running correctly. Writing anything to this register will clear the bits.

Field Name	Description
$MODE_{1-0}$	Mode Status: Reports which mode the sensor is in. 00 = Run 01 = Rest 1 10 = Rest 2 11 = Rest 3
OBS_{4-0}	Set every frame

Reserved **Address: 0x2f-0x39**

POWER_UP_RESET **Address: 0x3a**

Access: Write Reset Value: NA

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	RST_7	RST_6	RST_5	RST_4	RST_3	RST_2	RST_1	RST_0

Data Type : 8-bit integer

USAGE : Write 0x5a to this register to reset the chip. All settings will revert to default values. Reset is required after recovering from shutdown mode.

SHUTDOWN **Address: 0x3b**

Access: Write Only Reset Value: NA

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	SD_7	SD_6	SD_5	SD_4	SD_3	SD_2	SD_1	SD_0

Data Type : 8-bit integer

USAGE : Write 0xe7 to set the chip to shutdown mode, use POWER_UP_RESET register (address 0x3b) to power up the chip.

Reserved **Address: 0x3c-0x3d**

Inverse_Revision_ID **Address: 0x3e**

Access: Read Reset Value: 0xfc

Bit	7	6	5	4	3	2	1	0
Field	$NRID_7$	$NRID_6$	$NRID_5$	$NRID_4$	$NRID_3$	$NRID_2$	$NRID_1$	$NRID_0$

Data Type : Inverse 8-Bit unsigned integer

USAGE : This value is the inverse of the Revision_ID. It can be used to test the SPI port.

Inverse_Product_ID **Address: 0x3f**

Access: Read Reset Value: 0xdf

Bit	7	6	5	4	3	2	1	0
Field	$NPID_7$	$NPID_6$	$NPID_5$	$NPID_4$	$NPID_3$	$NPID_2$	$NPID_1$	$NPID_0$

Data Type : Inverse 8-Bit unsigned integer

USAGE : This value is the inverse of the Product_ID. It can be used to test the SPI port.

Motion_Burst **Address: 0x42**

Access: Read Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	MB_7	MB_6	MB_5	MB_4	MB_3	MB_2	MB_1	MB_0

Data Type : Various.

USAGE : Read from this register to activate burst mode. The sensor will return the data in the Motion register, Delta_X, Delta_Y, Squal, Shutter_Upper, Shutter_Lower, and Maximum_Pixel. Reading the first 3 bytes clears the motion data. The read may be terminated anytime after Delta_X is read.

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

Avago, Avago Technologies, and the A logo are trademarks of Avago Technologies in the United States and other countries.
Data subject to change. Copyright © 2005-2009 Avago Technologies. All rights reserved.
AV02-1451EN - July 7, 2009